**Lab 6**

**OBJECTIVES:**

* To learn and understand the working of different types of decoders
* To learn and understand how to design a multiple output combinational circuit using Decoders

**EQUIPMENT:** Logic trainer, Logic probe

**COMPONENTS:** ICs 74LS08, 74LS32, 74LS04, 74LS139

**2-to-4 line decoders:**

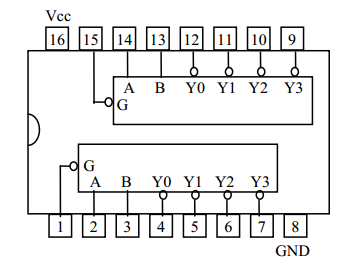
74LS139 IC contains two fully independent 2-to-4 line decoders with active low enables. The function table and connection diagram for this IC are shown below:

**Function Table:**

| **Enable** | **Selection Inputs** | | **Outputs** | | | |
| --- | --- | --- | --- | --- | --- | --- |
| **G** | **B** | **A** | **Y0** | **Y1** | **Y2** | **Y3** |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

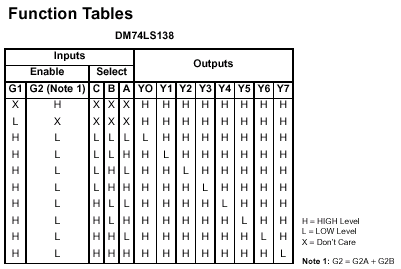
H= Logic High, L= Logic Low, X= Don’t Care

**Connection Diagram:**

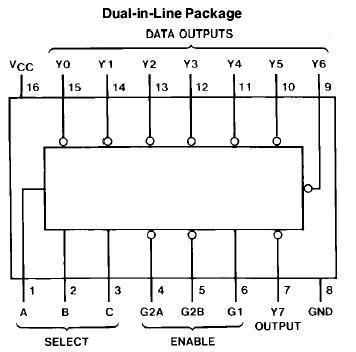
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**3-to-8 line decoders:**

74LS138 IC contains 3-to-8 line decoder. The function table and connection diagram for this IC are shown below:

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**Connection Diagram:**



**Lab Tasks:**

**Question 1 (Hardware Implementation):**

Make a truth table and implement **2x4 Decoder with a low enable** using **8 AND gates and 3 NOT gates.**

**Question 2 (Hardware Implementation):**

Implement 3x8 decoder using two **2x4 decoders and a NOT gate**

**Question 3:**

**4 bit parity Checker:** Implement on **Logic Works** a circuit that receives **4-bit message** and outputs **Error (E=1) if its parity is ODD**

**(Implement it using XOR and XNOR gates)**

**Question 4:**

Implement on **Logic Works** a doubler circuit. It takes a **3 bit input** and multiplies it by two and gives a **4 bit output.**

**(Implement it using XOR and XNOR gates)**